## 11.10 A UMTS-Compliant Fully Digitally Controlled Oscillator with 100Mhz Fine-Tuning Range in 0.13μm CMOS

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Frequency synthesizers, and especially phase locked loops (PLL), are fundamental blocks used in every RF wireless application. Continuous demand for high levels of integration and reduced power consumption can only be realistically achieved using a digital control system approach. One of the most critical blocks in a digital PLL design is the digitally-controlled oscillator (DCO). The function of a DCO is to generate a signal whose frequency is proportional to a digital word calculated by a digital loop filter.

DCOs for several communication standards have been analyzed in the literature [1,2,3,4,5] but none of them is suitable for the frequency division duplexing mode of UMTS because of the low power consumption required and the wide bandwidth of the output signal. If direct modulation of the RF signal is targeted, an extremely wide fine-tuning range is required. System simulations show that a fine-tuning range on the order of 100MHz is needed to achieve modulation. The approaches shown in [1], [2] based on ring oscillators, are not suitable for UMTS because they have large phase noise. The LC-oscillator-based DCOs described in [4] and [5] result in low phase noise, but their power consumption is too high for a continuously operating system. The solution presented in [3] has acceptable phase noise and low power consumption, but the fine-tuning range is not suitable to modulate a wideband signal. This paper presents the first fully digitally controlled oscillator suitable for UMTS applications implemented in a standard 0.13μm CMOS process with 6 metal layers. The oscillator has low power consumption and a wide fine-tuning range. For an output frequency of 2GHz, the system draws only 3.2mA in TX mode and 2.6mA in RX mode from a 2.5V supply, with a phase noise of -118dBc/Hz in TX mode and -115dBc/Hz in RX mode, both at 1 MHz offset. A wide course-tuning range, from 3.45 to 4.45GHz, is needed to cover all UMTS bands and is achieved using a binary-weighted switched capacitor bank. A wide fine-tuning range of more than 100MHz with discrete fine-frequency steps of 200kHz maximum is achieved by a thermometer-coded varactor bank. Figure 11.10.1 summarizes all the points described above. According to this comparison, the DCO presented here has significantly smaller chip area and a wider fine-tuning range, which put this work well beyond the current state of the art. All these characteristics enable the realization of a fully digital phase path for a polar transmitter.

The complete schematic of the DCO is shown in Fig. 11.10.2. Cross-coupled transistors $M_1$ and $M_2$ provide the negative resistance necessary to compensate the losses in the LC tank and sustain oscillations. The LC tank consists of a switchable binary-weighted capacitor bank and a thermometer-coded varactor bank in parallel with an inductor. The binary-weighted capacitor bank is used to achieve the coarse-frequency tuning range necessary to cover all the UMTS bands and is implemented with eight pairs of metal-insulator-metal capacitors connected in series through NMOS transistors.

The fine-frequency tuning necessary for modulation is achieved by connecting a bank of varactors in parallel with the tank. The maximum capacitance variation with the minimum parasitic capacitance was achieved using PMOS varactors with dimensions optimized for the target technology. In order to optimize the layout area, the varactor bank was organized in a matrix of elementary cells as shown in Fig. 11.10.3. Each cell consists of two varactors with shorted drain and source terminals and a logic decoder. Depending on the row and column information, the decoder sets the voltage on the drain-source terminal of the varactors either to a fixed potential or to ground. Due to resistors $R_c$, which set the DC potentials of the gates to ground, and the AC coupling $C_c$, when the drain-source potential is set to ground each pair of varactors behaves like a small capacitor, while in the other case they behave like a large capacitor. DCO fine tuning is controlled by a 10b digital word. After a conversion from binary weighted to thermometer coded, the tuning information is latched to avoid glitches. Local logic implemented in the matrix decodes the row and column information in such a way that each odd column is filled up from row 1 to row $n$, while each even column is filled up from row $n$ back to row 1 of the matrix. This "serpentine" topology ensures both a good matching between each element and a lower influence coming from variations of process and temperature. The current required to bias the DCO core is provided by the current source built with PMOS transistors $M_3$ and $M_4$. With this topology, a static pushing figure of less than 1MHz/V at the DCO frequency can be achieved. A low-frequency filter consisting of $R_f$ and $C_f$ ensures low phase noise for offset frequencies higher than 10kHz. A tail coil suppresses effects coming from the second harmonic, which can increase noise for frequencies far from the carrier [6].

Figure 11.10.4 shows the DCO coarse-tuning characteristic versus the coarse-tuning word after a divide-by-2 operation. Under nominal conditions, a 25% tuning range can be achieved. Note that the tuning curves follow the typical $1/\sqrt{LC}$ law. Figure 11.10.5 shows the fine-tuning characteristic versus the fine-tuning word for minimum, typical and maximum frequencies of operation. As expected, the higher the carrier frequency, the larger the fine-tuning step. Several big jumps can be noticed for tuning words related to multiples of 32 (32-64-96…) because of the fact that each row is built up of 32 elements. This behavior can be explained noting that for those values, the active varactors are always at the border of the matrix and matching problems arise. The use of dummy cells can improve this side effect.

The open-loop measured phase noise for the DCO with a 2GHz carrier frequency is shown in Fig. 11.10.6.

A micrograph of the 0.19 mm$^2$ chip, including DCO core and biasing block, is shown in Fig. 11.10.7.

*References:*

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[2] J. Dunning et al., "An All-Digital Phase-Locked-Loop with 50-cycle Lock Time Suitable for High Performance Microprocessors," *IEEE J. Solid-State Circuits*, vol 30, pp. 412-422, Apr., 1995.
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| DCO | Tech. [nm] | Phase noise [dBc/Hz] | Fine Tuning Range [MHz] | Coarse Tuning Range [GHz] | Current [mA] | Die Area [mm²] |
|---|---|---|---|---|---|---|
| [3] | 130 | -112@500kHz (1) | 0.32 | 0.5 | 2.3 | 0.54 |
| [4] | 90 | -165@20MHz (2) | 0.768 | 0.9 | 18 | N/A |
| [5] | 130 | -120@1MHz (1) | 1 | 0.7 | 16 | 0.24 |
| (this) | 130 | -118@1MHz (1) | 100 | 1 | 2.3 | 0.19 |

(1): Phase noise measured at carrier frequency 2 GHz

(2): Phase noise measured for GSM 900 MHz

**Figure 11.10.1: Comparison with the state of the art.**

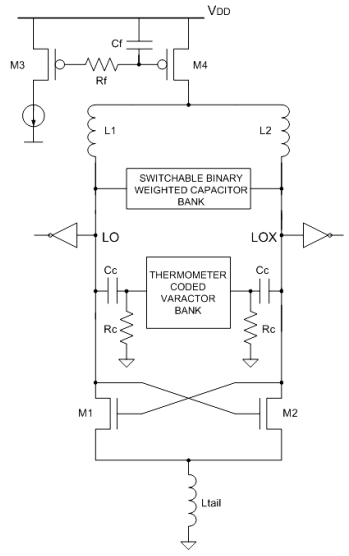



**Figure 11.10.2: Complete DCO schematic.**



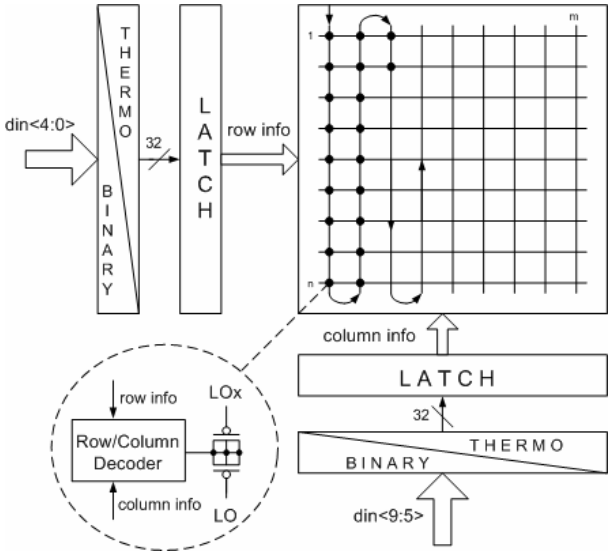



**Figure 11.10.3: Varactor bank implementation.**

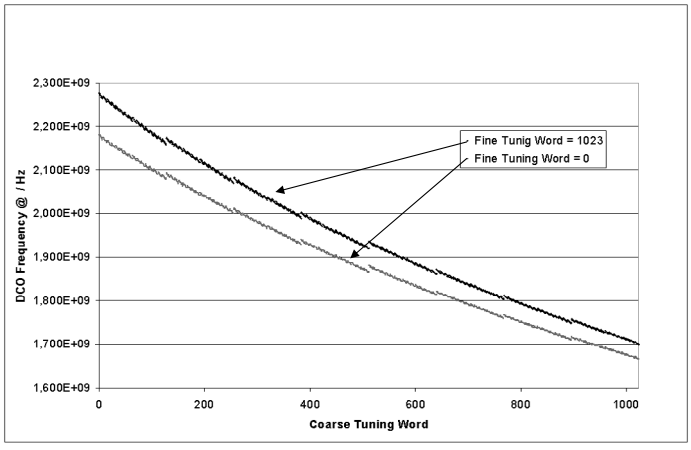
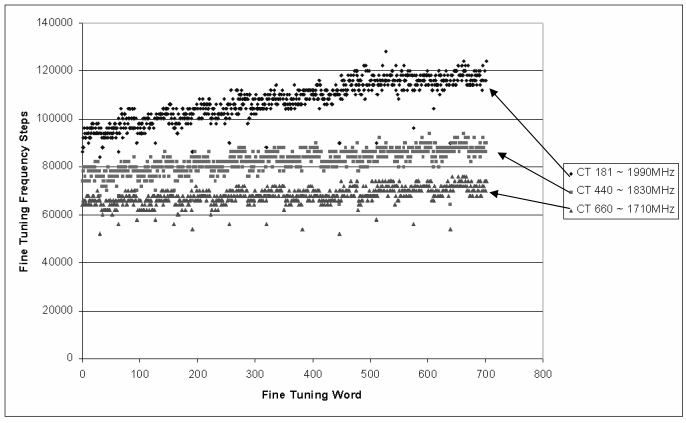



**Figure 11.10.4: Coarse tuning step versus coarse tuning word.**




**11.10.5: Fine tuning step versus fine tuning word.**

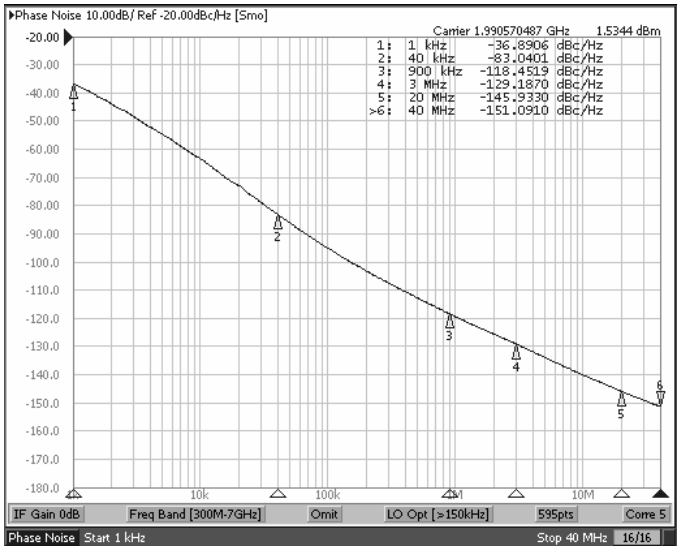



**Figure 11.10.6: Measured phase noise.**

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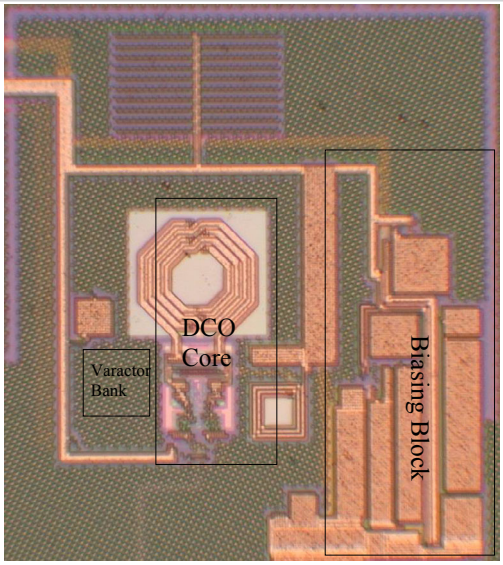


**Figure 11.10.7: Die micrograph.**

 